IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) ~~Integrated~~ An integrated circuit ~~having~~ comprising:

a plurality of processing modules ~~(M, S) and~~ including a first module and a second module;

an interconnect ~~means (N)~~ device for coupling said plurality of processing modules ~~(M, S)~~ and for enabling a device-level communication based on transactions between said plurality of processing modules ~~(M, S)~~, wherein ~~at least one~~ the first processing module ~~(M)~~ issues at least one transaction ~~towards at least one~~ for reception by the second processing module ~~(S) comprising:~~ through the interconnect device;

at least one transaction abortion unit ~~(TAU)~~ connected at least one of between the first module and the interconnect device

and between the second module and the interconnect device for aborting at least one transaction issued from said first module ~~by~~ in response to receiving an abort request ~~(abt)~~ issued by said first module ~~(M)~~, by initiating a discard of said at least one transaction to be aborted, and by issuing a response ~~(abt_ack)~~ indicating ~~the~~ a success/failure of the ~~requested transaction abortion~~ abort request; and

at least one network interface associated to one of said plurality of processing modules for controlling the communication between said one of said plurality of processing modules and said interconnect,

wherein said at least one transaction abortion unit is arranged in one of said network interfaces;

wherein said at least one network interface further comprise a request buffer for buffering received data; and

wherein said transaction abortion unit is adapted to issue a discard for said at least one transaction to be aborted as stored in said request buffer.

Claim 2 (Canceled)

3.(Currently Amended) ~~Integrated~~ The integrated circuit according to ~~claim 2~~ claim 1, wherein

said at least one transaction abortion unit ~~(TAU)~~ is adapted to perform said at least one transaction abortion atomically or partially.

Claim 4 (Canceled)

5.(Currently Amended) ~~Integrated circuit according to claim 2, wherein~~ An integrated circuit comprising:

a plurality of processing modules including a first module and a second module;

an interconnect device for coupling said plurality of processing modules and for enabling a device-level communication based on transactions between said plurality of processing modules, wherein the first processing module issues at least one transaction for reception by the second processing module through the interconnect device;

at least one transaction abortion unit connected at least one

of between the first module and the interconnect device and between the second module and the interconnect device for aborting at least one transaction issued from said first module in response to receiving an abort request issued by said first module, by initiating a discard of said at least one transaction to be aborted, and by issuing a response indicating a success/failure of the abort request; and

at least one network interface associated to one of said plurality of processing modules for controlling the communication between said one of said plurality of processing modules and said interconnect,

wherein said at least one transaction abortion unit is arranged in one of said network interfaces;

wherein said at least one network interface ~~(NI)~~ further comprise a response buffer ~~(RESP)~~ for buffering outgoing ~~data,~~ data; and

wherein said transaction abortion unit ~~(TAU)~~ is adapted to issue a discard for said at least one transaction to be aborted as stored in said response buffer ~~(RESP)~~.

6.(Currently Amended) ~~Integrated circuit according to claim 1, wherein~~ An integrated circuit comprising:

a plurality of processing modules including a first module and a second module;

an interconnect device for coupling said plurality of processing modules and for enabling a device-level communication based on transactions between said plurality of processing modules, wherein the first processing module issues at least one transaction for reception by the second processing module through the interconnect device; and

at least one transaction abortion unit connected at least one of between the first module and the interconnect device and between the second module and the interconnect device for aborting at least one transaction issued from said first module in response to receiving an abort request issued by said first module, by initiating a discard of said at least one transaction to be aborted, and by issuing a response indicating a success/failure of the abort request;

wherein said request for said at least one transaction abortion specifies which transactions are to be aborted, and

wherein said response ~~(abt_ack)~~ issued by said transaction abortion unit ~~(TAU)~~ specifies which of the requested at least one transaction have been aborted.

7.(Currently Amended) ~~Method~~ A method for transaction abortion in an integrated circuit having a plurality of processing modules ~~(M, S)~~ and an interconnect ~~means (N)~~ device for coupling said plurality of processing modules ~~(M, S)~~ and for enabling a ~~device-level~~ communication based on transactions between said plurality of processing modules ~~(M, S)~~, wherein ~~at least one~~ a first processing module ~~(M)~~ issues at least one transaction towards ~~at least one~~ a second processing module ~~(S)~~, the method comprising the ~~step~~ acts of:

buffering received data in a request buffer of a network interface configured to control the communication between said first processing module and said interconnect device;

aborting at least one transaction issued from said first module by receiving an abort request ~~(abt)~~ issued by said first module ~~(M)~~, by initiating a discard of said at least one transaction to be aborted, and by issuing a response ~~(abt_ack)~~

indicating the success/failure of the requested transaction abortion; and

issuing a discard for said at least one transaction to be aborted as stored in said request buffer.

8. (Currently Amended) ~~Data~~ A data processing system, comprising:

a plurality of processing modules ~~(M, S) and~~ including a first module and a second module;

an interconnect ~~means (N)~~ device for coupling said plurality of processing modules ~~(M, S)~~ and for enabling a device-level communication based on transactions between said plurality of processing modules ~~(M, S)~~, wherein ~~at least one~~ the first processing module ~~(M)~~ issues at least one transaction ~~towards at least one~~ for reception by the second processing module ~~(S) comprising:~~ through the interconnect device;

at least one transaction abortion unit ~~(TAU)~~ connected at least one of between the first module and the interconnect device and between the second module and the interconnect device for aborting at least one transaction issued from said first module ~~by~~

in response to receiving an abort request ~~(abt)~~ issued by said first module ~~(M)~~, by initiating a discard of said at least one transaction to be aborted, and by issuing a response ~~(abt_ack)~~ indicating ~~the~~ a success/failure of the ~~requested transaction abortion~~ abort request; and

at least one network interface associated to one of said plurality of processing modules for controlling the communication between said one of said plurality of processing modules and said interconnect,

wherein said at least one transaction abortion unit is arranged in one of said network interfaces;

wherein said at least one network interface further comprise a request buffer for buffering received data; and

wherein said transaction abortion unit is adapted to issue a discard for said at least one transaction to be aborted as stored in said request buffer.

9.(New) A method for transaction abortion in an integrated circuit having a plurality of processing modules and an interconnect device for coupling said plurality of processing

modules and for enabling a communication based on transactions between said plurality of processing modules, wherein a first processing module issues at least one transaction towards a second processing module, the method comprising the acts of:

buffering outgoing data in a response buffer of a network interface configured to control the communication between said first processing module and said interconnect device;

aborting at least one transaction issued from said first module by receiving an abort request issued by said first module, by initiating a discard of said at least one transaction to be aborted, and by issuing a response indicating the success/failure of the requested transaction abortion; and

issuing a discard for said at least one transaction to be aborted as stored in said response buffer.

10.(New) A method for transaction abortion in an integrated circuit having a plurality of processing modules and an interconnect device for coupling said plurality of processing modules and for enabling a communication based on transactions between said plurality of processing modules, wherein a first

processing module issues at least one transaction towards a second processing module, the method comprising the acts of:

issuing by said first module an abort request that specifies which transactions are to be aborted; and

aborting at least one transaction issued from said first module in response to receiving the abort request, by initiating a discard of said at least one transaction to be aborted, and by issuing a response indicating the success/failure of the requested transaction abortion; wherein the response indicating the success/failure indicates which of the transactions have been aborted.